A 2.7-V SiGe HBT Variable Gain Amplifier for CDMA Applications

Chang-Woo Kim, *Member, IEEE,* and Young-Gi Kim

***Abstract*—A monolithic SiGe HBT variable gain amplifier with high dB-linear gain control and high linearity has been developed for CDMA applications. The VGA achieves a 30-dB dynamic gain control with a control range of 0–2.7 Vdc in 824–849 MHz band. The maximum gain and attenuation are 23 dB and 7 dB, respectively. Input/output VSWRs keep low and constant despite change in the gain-control voltage. At a low operation voltage of 2.7 V, the VGA produces a 1-dB compression output power of 13 dBm and ±885-kHz ACPR of −57 dBc at a 5-dBm output power.**

***Index Terms*—CDMA, SiGe HBT, variable gain amplifier (VGA).**

I. Introduction

CODE DIVISION MULTIPLE ACCESS (CDMA) phones need careful regulation of signal levels on both up and down streams. A transmitter of the phone provides a signal with well-defined output power level to upstream circuits so that it does not dominate the input spectrum at the base station. Thus, the transmitter requires a variable gain amplifier (VGA) with wide and high dB-linear gain control and high linearity characteristics.

There are several monolithic VGAs combined with GaAs technologies for CDMA applications [1]–[3]. The GaAs-based ICs are relatively expensive, so low-cost VGAs are required substantially since cost is of major concern for all wireless communication products. This can be satisfied by advanced SiGe heterojunction bipolar transistor (HBT) technologies.

In this work, we have developed a monolithic SiGe VGA with a high dB-linear gain control and high linearity. The VGA was designed and fabricated by using ASB's SiGe MMIC design libraries and Tachyonics's SiGe HBT technology. The VGA was measured for small signal and large signal performances. Large signal measurements were performed under single-tone and digitally modulated signal inputs. The measured results will be discussed.

II. MMIC Design and Fabrication

Fig. 1 shows the measured *I-V* output characteristics for SiGe HBTs with a $1 \times 4\ \mu\mathrm{m}^2$ emitter area. The HBTs demonstrate a dc gain of 160 with $\mathrm{BV_{CEO}} = 8\ \mathrm{V}$. The cutoff frequency $(\mathrm{f_t})$ and maximum oscillation frequency $(\mathrm{f_{max}})$ as a function of the collector-current are shown in Fig. 2. The peak $\mathrm{f_t}$ and $\mathrm{f_{max}}$ are 30 and 53 GHz, respectively. A detailed description of structure and fabrication process for the SiGe HBTs can be found in [4].

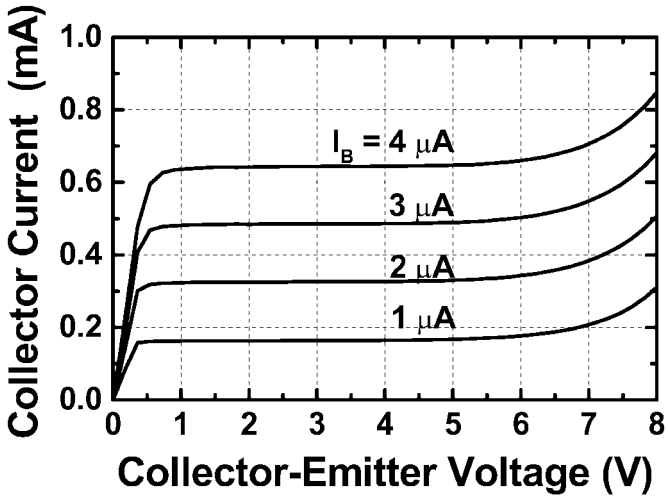

Fig. 1. Measured *I-V* output characteristics for SiGe HBTs.

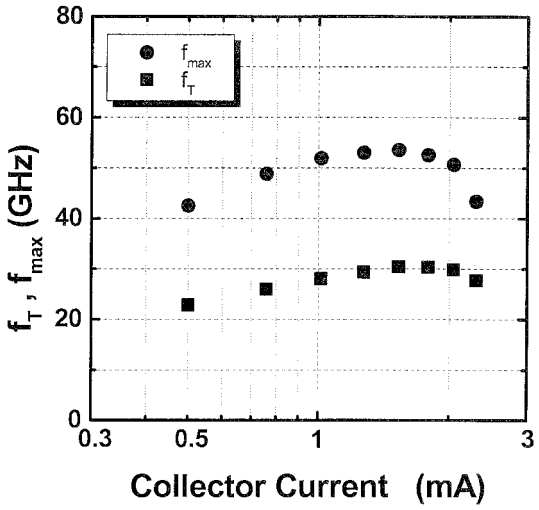

Fig. 2. Measured dependence of cutoff frequency $\mathrm{f_t}$ and maximum oscillation frequency $\mathrm{f_{max}}$ on collector current at $\mathrm{V_{CE}} = 5\ \mathrm{V}$.

A simplified schematic of the designed VGA is shown in Fig. 3. Two types of multifinger HBTs were used in the circuit; two HBTs with five emitter-fingers were used for the first and second stages ($\mathrm{Q_1}$ and $\mathrm{Q_2}$) and a 20-finger HBT was used for the 3rd stage $(\mathrm{Q_3})$. Each emitter-finger area is $1 \times 8\ \mu\mathrm{m}^2$ and the emitter-finger areas of the HBTs have been determined to satisfy the output power and linearity requirements. All MIM

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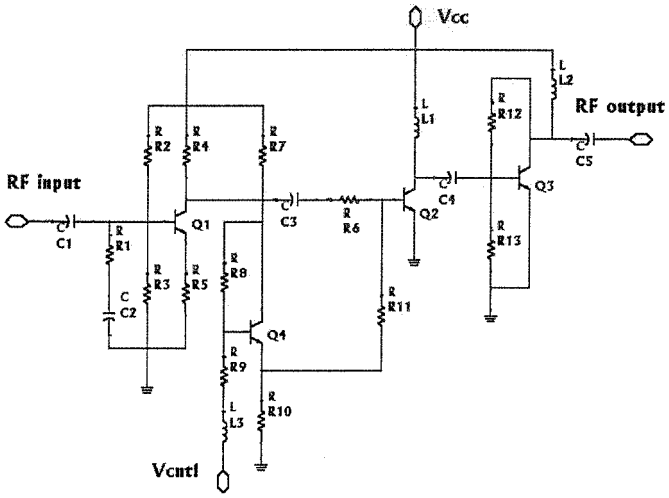

Fig. 3. Schematic circuit diagram of the VGA.

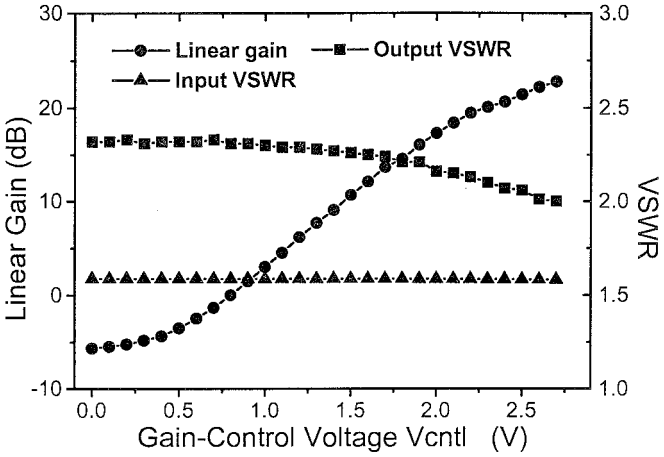

Fig. 5. Small-signal gain and input/output VSWR characterstics of the VGA as a function of gain-control voltage V_{cntl} at 835 MHz.

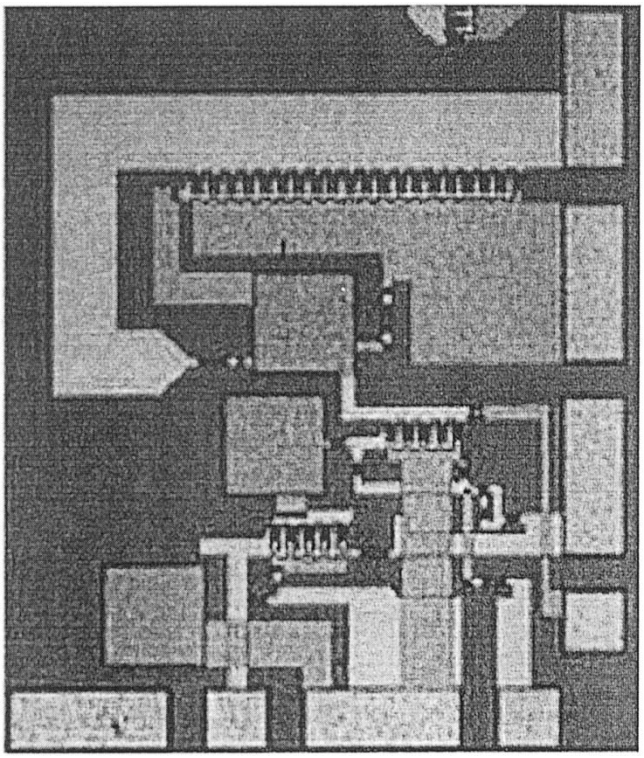

Fig. 4. Microphotograph of the VGA chip.

capacitors and thin film resistors were custom designed for this chip.

The VGA consists of three stages in a cascade connection. The 1st stage has been designed to be a kind of a buffer circuit without the gain so that the input VSWR keeps constant with varying the control voltage V_{cntl} of the 2nd stage. The 2nd stage provides the variable gain mechanism. The gain control is achieved by varying the base bias current (I_B) of Q_2 through controlling of the base voltage (V_{cntl}) of the emitter follower Q_4. The I_B is determined by $R_{10}I_E/R'$ where I_E is the emitter current of Q_4 and $R' = R_{10} + R_{11} + R_{BE}$ of Q_2. As V_{cntl} increases linearly, the gain of Q_2 increases dB-linearly. A feedback network (R_8) is used for bias stability. The 3rd stages acts as a fixed gain output buffer to amply the RF signal. A shunt feedback scheme is employed to reduce nonlinear distortion and instability. The resistors R_1, R_6, and R_{13} are used for an improvement of the amplifier's stability.

Using the Gummel-Poon model, the small and large signal simulations have been performed by Agilent's Advanced Design System (ADS) according to harmonic balance and envelope modulation analyzes. All passive elements have been optimized to obtain a linear power gain $\geq$25 dB, gain control range $\geq$30 dB, input VSWR $\leq$1.5, 1-dB compression output power $(P_{1-dB}) \geq 13$ dBm, and adjacent channel power ratio (ACPR) at $\pm$885-kHz offset bands ≤ -60 dBc in 824–849 MHz band (IS-95 CDMA frequency band of Korea). A microphotograph of the developed VGA chip is shown in Fig. 4. The MMIC chip was fabricated using Tachyonic's SiGe HBT foundry IC process. The chip size is $1 \times 1.2\ \text{mm}^2$.

III. Measurement Results

For small and large signal measurements under single-tone and digitally modulated signal inputs, the VGA chip was mounted chip-on-board (FR-4 test board) with off-chip surface mount components for choke, RF coupling, and output matching networks. The results were obtained from a 50-ohm measurement system.

Fig. 5 shows the measured gain control and input/output VSWR performance at 835 MHz (center frequency of Korean CDMA band). A dynamic gain control range of 30 dB is achieved by controlling V_{cntl} with a range from 0.0 to 2.7 V. The maximum gain of 23 dB is obtained at $V_{cntl} = 2.7$ V. The advantage of this scheme is that it can achieve a wide gain-control voltage range. In general, a gain-control voltage for 1-dB control in a bipolar transistor is much larger than a thermal voltage (26 mV/dB at the room temperature) in order to be insensitive to temperature variation. The VGA exhibits a gain-control voltage of 50 mV/dB. The input VSWR keeps low (< 1.6) and constant despite change in the gain-control voltage. The output return loss (9 dB) variation is less than 1-dB peak-to-peak over the gain-control range.

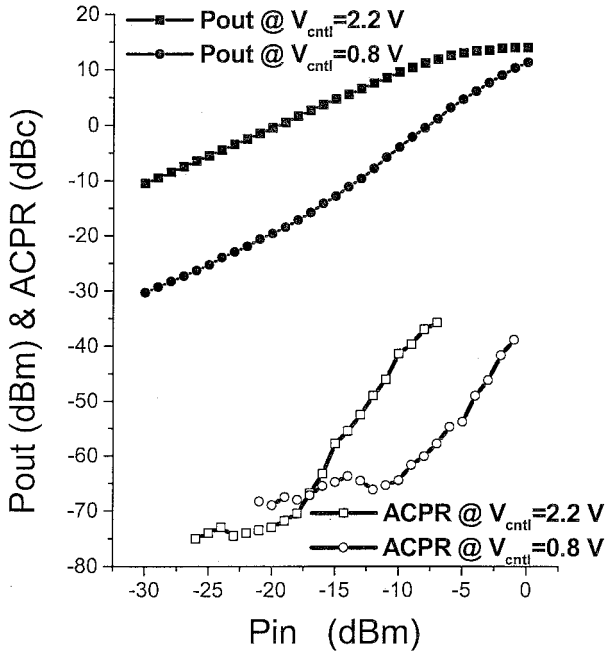

Fig. 6. Output power and adjacent channel power ratio (ACPR) at ±885 kHz offset bands characteristics versus input power of the VGA for various gain-control voltages at 835 MHz.

Fig. 6 shows the output power and adjacent channel leakage power ratio (ACPR) characteristics as a function of the input power for two conditions with high ($@\mathrm{V_{cntl}} = 2.2\ \mathrm{V}$) and low ($@\mathrm{V_{cntl}} = 0.8\ \mathrm{V}$) gains. At $\mathrm{V_{cntl}} = 2.2\ \mathrm{V}$, the VGA produces a $\mathrm{P_{1-dB}}$ of 13 dBm with a 20-dB linear power gain and; at $\mathrm{V_{cntl}} = 0.8\ \mathrm{V}$, the VGA produces a $\mathrm{P_{1-dB}}$ of 12 dBm with a 0-dB linear power gain. For a 5-dBm output power, −57-dBc ACPR at ± 885-kHz offset bands is obtained at $\mathrm{V_{cntl}} = 2.2\ \mathrm{V}$, while −52-dBc ACPR is obtained at $\mathrm{V_{cntl}} = 0.8\ \mathrm{V}$. As the power gain decreases with $\mathrm{V_{cntl}}$, the ACPR becomes degraded, but keeps lower than −60 dBc below 0-dBm ouput power. The amplifier has been operated at class AB with a collector current of 34 mA.

IV. Conclusion

We have developed a monolithic SiGe HBT VGA with a high dB-linear gain control and high linearity. Our work addressed one of major challenges for the implementation of fully monolithic transmitters using silicon technology. The experimental results indicate that SiGe HBT VGAs have high potential in CDMA phones with reducing chip cost.

Acknowledgment

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